IN THE CLAIMS

Please amend the claims to read as follows:

Listing of Claims

Claims 1-13 (Cancelled).

14. (New) An AGC circuit comprising:

a variable gain amplifier circuit that gain controls, in accordance with a gain control signal, an input signal to produce a gain controlled output signal;

a rectification circuit that rectifies the gain controlled output signal to produce a rectified signal;

a voltage comparator that compares the rectified signal with a preset voltage to produce a comparator output voltage;

an up/down counter that switches, in accordance with the comparator output voltage, between an up-count operation and a down-count operation to produce a count value; and

a D/A conversion circuit that outputs an analog voltage corresponding to the count value, wherein:

the count value is produced in accordance with first and second clock signals, provided respectively to first and second input terminals of the up/down counter, such that:

when the up-count operation is performed, the up/down counter increments the count value in accordance with the first clock signal; and

when the down-count operation is performed, the up/down counter decrements the count value in accordance with the second clock signal, and

the gain control signal provided to the variable gain amplifier circuit corresponds to the analog voltage output from the D/A conversion circuit.

15. (New) The AGC circuit of claim 14, wherein the up-count and down-count operations are regulated such that the count value is restricted within a range from an upper limit to a lower limit.

16. (New) An AGC circuit comprising:

a variable gain amplifier circuit that gain controls, in accordance with a gain control signal, an input signal to produce a gain controlled output signal;

a rectification circuit that rectifies the gain controlled output signal to produce a rectified signal;

a voltage comparator that compares the rectified signal with a preset voltage to produce a comparator output voltage;

a register that stores, according to a cycle of a reference clock, the comparator output voltage so as to generate a register output signal that does not reflect changes of the comparator output voltage occurring at times other than a synchronization time of the reference clock;

an up/down counter that switches, in accordance with the register output signal, between an up-count operation and a down-count operation to produce a count value; and

a D/A conversion circuit that outputs an analog voltage corresponding to the count value, wherein:

the gain control signal provided to the variable gain amplifier circuit corresponds to the analog voltage output from the D/A conversion circuit.

17. (New) An AGC circuit comprising:

a variable gain amplifier circuit that gain controls, in accordance with a gain control signal, an input signal to produce a gain controlled output signal;

a rectification circuit that rectifies the gain controlled output signal to produce a rectified signal;

a voltage comparator that compares the rectified signal with a preset voltage to produce a comparator output voltage;

a count operation control circuit that conveys or inhibits conveyance of the comparator output voltage in accordance with a count value;

an up/down counter that switches, in accordance with the conveyed comparator output voltage, between an up-count operation and a down-count operation to produce the count value; and

a D/A conversion circuit that outputs an analog voltage corresponding to the count value, wherein:

the count operation control circuit controls the conveyance of the comparator output voltage, controlling the up-count and down-count operations, so as to restrict the count value within a range from an upper limit to a lower limit, and

the gain control signal provided to the variable gain amplifier circuit corresponds to the analog voltage output from the D/A conversion circuit.

18. (New) An AGC circuit comprising:

a variable gain amplifier circuit that gain controls, in accordance with a gain control signal, an input signal to produce a gain controlled output signal;

a rectification circuit that rectifies the gain controlled output signal to produce a rectified signal;

a voltage comparator that compares the rectified signal with a preset voltage to produce a comparator output voltage;

a register that stores, according to a cycle of a reference clock, the comparator output voltage so as to generate a register output signal that does not reflect changes of the comparator output voltage occurring at times other than a synchronization time of the reference clock;

a count operation control circuit that conveys or inhibits conveyance of the register output signal in accordance with a count value;

an up/down counter that switches, in accordance with the conveyed register output signal, between an up-count operation and a down-count operation to produce the count value; and

a D/A conversion circuit that outputs an analog voltage corresponding to the count value, wherein:

the count operation control circuit controls the conveyance of the register output signal, controlling the up-count and down-count operations, so as to restrict the count value within a range from an upper limit to a lower limit, and

the gain control signal provided to the variable gain amplifier circuit corresponds to the analog voltage output from the D/A conversion circuit.

19. (New) An AGC circuit comprising:

a variable gain amplifier circuit that gain controls, in accordance with a gain control signal, an input signal to produce a gain controlled output signal;

a rectification circuit that rectifies the gain controlled output signal to produce a rectified signal;

a first voltage comparator that compares the rectified signal with a preset voltage to produce a first comparator output voltage;

a first up/down counter that switches, in accordance with the first comparator output voltage, between an up-count operation and a down-count operation to produce a first count value;

a first D/A conversion circuit that outputs a first analog voltage corresponding to the first count value;

a second up/down counter that switches, in accordance with a control signal, between an up-count operation and a down-count operation to produce a second count value;

a second D/A conversion circuit that outputs a second analog voltage corresponding to the second count value;

a second voltage comparator that compares the first and second analog voltages to produce the control signal; and

a changeover circuit that selects, based on the control signal, the one of the first and second analog signals having the greater voltage, wherein

the gain control signal provided to the variable gain amplifier circuit corresponds to the selected one of the first and second analog signals output from the changeover circuit.

20. (New) The AGC circuit of claim 19, wherein:

a first up-count operation clock and a first down-count operation clock are input separately to the first up/down counter; and

a second up-count operation clock and a second down-count operation clock are input separately to the second up/down counter.

21. (New) The AGC circuit of claim 19, further comprising:

a first register that stores, according to a cycle of a first reference clock, the first comparator output voltage so as to generate a first register output signal that does not reflect changes of the first comparator output voltage occurring at times other than a synchronization time of the first reference clock, wherein:

the first up/down counter switches, in accordance with the first register output signal, between the up-count operation and the down-count operation to produce the first count value.

22. (New) The AGC circuit of claim 21, further comprising:

a second register that stores, according to a cycle of a second reference clock, the control signal so as to generate a second register output signal that does not reflect changes of the control signal occurring at times other than a synchronization time of the second reference clock, wherein:

the second up/down counter switches, in accordance with the second register output signal, between the up-count operation and the down-count operation to produce the second count value.

23. (New) The AGC circuit of claim 22, further comprising:

a first count operation control circuit that, in accordance with the first count value, conveys or inhibits conveyance of the first register output signal to the first up/down counter so as to regulate the up-count and down-count operations of the first up/down counter in accordance with the conveyed first register output signal; and

a second count operation control circuit that, in accordance with the second count value, conveys or inhibits conveyance of

the second register output signal to the second up/down counter so as to regulate the up-count and down-count operations of the second up/down counter in accordance with the conveyed second register output signal, wherein:

the first count operation control circuit controls the conveyance of the first register output signal, controlling the up-count and down-count operations of the first up/down counter, so as to restrict the first count value within a range from a first upper limit to a first lower limit, and

the second count operation control circuit controls the conveyance of the second register output signal, controlling the up-count and down-count operations of the second up/down counter, so as to restrict the second count value within a range from a second upper limit to a second lower limit.

24. (New) The AGC circuit of claim 19, further comprising:

a first count operation control circuit that, in accordance with the first count value, conveys or inhibits conveyance of the first comparator output voltage to the first up/down counter so as to regulate the up-count and down-count operations of the first up/down counter in accordance with the conveyed first comparator output voltage; and

a second count operation control circuit that, in accordance with the second count value, conveys or inhibits conveyance of the control signal to the second up/down counter so as to regulate the up-count and down-count operations of the second up/down counter in accordance with the conveyed control signal, wherein:

the first count operation control circuit controls the conveyance of the first comparator output voltage, controlling the up-count and down-count operations of the first up/down counter, so as to restrict the first count value within a range from a first upper limit to a first lower limit, and

the second count operation control circuit controls the conveyance of the control signal, controlling the up-count and down-count operations of the second up/down counter, so as to restrict the second count value within a range from a second upper limit to a second lower limit.

25. (New) The AGC circuit of claim 19, wherein:

the up-count and down-count operations of the first up/down counter are regulated such that the first count value is restricted within a range from a first upper limit to a first lower limit; and

the up-count and down-count operations of the second up/down counter are regulated such that the second count value is restricted within a range from a second upper limit to a second lower limit.